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10/052,700	01/17/2002	Mark Sandford	LS/0014.01	1376

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EXAMINER	
NGUYEN, HAU H	

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2676	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/052,700	Applicant(s) SANDFORD, MARK	
	Examiner Hau H Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-4, 6-11, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by Baddiley (U.S. Patent No. 4,852,065).

Referring to claims 1, 2, 8, and 10, Baddiley teaches a data reorganization apparatus comprising: a buffer store having a width equal to p x q bit positions, these positions being logically arranged in rows and columns with p bits per row and q bits per column (matrix in orthogonal direction); input means for writing (storing) each p-bit group into a selected row of bit positions in the buffer store; output means for reading (retrieving) a succession of q-bit groups from selected columns of bit positions in the buffer store (col. 1, lines 45-60).

In regard to claim 3, as shown in Fig. 2, Baddiley depicts a plurality of address buses in the row direction, and a plurality of buses in the column direction.

Referring to claim 4, as described in column 3, lines 3-14, Badiley teaches the image information comprises pixel values.

In regard to claims 6 and 7, Baddiley teaches each pixel may be encoded as a single bit (for black-and-white images) or as a plurality of bits (for grey-scale or colour images) (col. 2, lines 64-66), thus, including 16-bit pixels.

Referring to claims 9, 11, and 13, Baddiley teaches when writing to the buffer 20, bits A5,A6 come from the least significant end of counter 40, bits A0-A4 from the middle, and bits W0,W1,W2,A7,A8 from the most significant end (col. 5, lines 30-34), and when reading from the buffer, the bits A7,A8 are derived from the least significant end of the counter 41, bits A0-A4 from the middle, and bits S0,S1,S2,A5,A6 from the most significant end (col. 5, lines 49-52).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 16-18, 20-30, 32-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Okuno (U.S. Patent No. 6,105,114).

Referring to claims 1, 16, 18, 21-24, Okuno teaches a memory system as shown in Fig. 5, comprising a memory cell array 2, an address translation circuit 5 coupled to a row decoder 3 and column decoder 4. As shown in Figs. 8A and 8B, Okuno teaches if data of an output array of a pre-stage DCT is written (stored) into each memory cell 9 shown in FIG. 8A in the order as shown by an arrow 10 (row/horizontal direction), an array required as an array for a post-stage DCT input is obtained by reading (retrieving) in the order shown by an arrow 11 of FIG. 8B (column/vertical direction). On the other hand, if a data block is written (stored) in the order shown by arrow 11 of FIG. 8B (column/vertical direction), an array desired as a post-stage DCT input is the one obtained by reading (retrieving) in the order shown by arrow 10 of FIG. 8A (row/horizontal direction) (col. 8, lines 28-36).

Referring to claim 17, Okuno teaches a flip-flop connecting to each memory element corresponding to an address in the memory array as shown in Fig. 13 (col. 11, lines 1-7).

In regard to claim 20, Okuno teach memory cell array 2 having 8 x 8 memory cells, and address signal supplied to the memory cell array is 6 bits (col. 8, lines 49-51), thus the two-dimensional array is symmetrical.

As for claims 25 and 26, Okuno teaches an address of each memory cell is represented by (row address, column address) as shown in FIG. 9 (col., lines 63-65), and address signal ADR supplied to address translation circuit 5 is 6 bits (col. 8, lines 49-51).

In regard to claims 27 and 29, Okuno teach the memory system 8 has a configuration of 2-port memory (for input and output) (col. 8, lines 39-40).

In regard to claims 28, 30, and 32, with reference again to Fig. 5, it is inherent that data inputs and data outputs should include buses for transferring data.

Referring to claims 33 and 34, as shown in Figs. 8A and 8B, it can be inferred that pixel values are processed in either sequential value or non-sequential value. Thus, pixel values along the arrow are sequential and pixel values outside the arrow are non-sequential.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Baddiley (U.S. Patent No. 4,852,065).

Referring to claim 5, although Baddiley does not teach the memory comprises static random access memory (SRAM), SRAM is well known in the art, and therefore, it would have been obvious to modify the memory array using RAM as taught by Baddiley by using SRAM so that performance of accessing memory is faster.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno (U.S. Patent No. 6,105,114).

Referring to claim 19, it would have been a matter of design choice to modify the number of memory array cells as taught by Okuno in one direction (horizontal or vertical) to be greater than the number of memory cells in the other direction so that the bit width of the memory array in one direction is not equal to the bit width of the memory array in the other direction, since applicant has not disclosed that different bit widths in each direction of the memory array solves any stated problem or is for any particular purpose and it appears that the above modification of the memory array as taught by Okuno would function equally well.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baddiley (U.S. Patent No. 4,852,065) in view of Clark et al. (U.S. Patent No. 6,603,814).

Referring to claim 12, as cited above, Baddiley teaches all the limitations of claim 12, except that data word is converted from 2's complement to a sign plus magnitude representation.

However, Clark et al. teach a method for storing video data, wherein as shown in Fig. 2, video signals 202, a discrete wavelet transform 204 block. The video compressor 200 also comprises a signed magnitude converter 210. In practice, the wavelet coefficients are stored in the input storage area 206 using a data representation that is most conducive to simple math operations, e.g., a one's complement or two's complement data representation. The signed

magnitude converter 210, in conjunction with the ADK compressor 208, converts the data stored in the input storage area 206 into a signed magnitude format (col. 5, lines 58-67, and col. 6, lines 1-3).

Therefore, it would have been obvious to one skilled in the to utilize the method as taught by Clark et al. in combination with the method as taught by Baddiley in order to avoid picture degradation (col. 2, lines 55-58).

9. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baddiley (U.S. Patent No. 4,852,065) in view of Rezeanu (U.S. Patent No. 6,567,884).

Referring to claims 14 and 15, as applied to claim 1 above, Baddiley teach all the limitations of claims 14 and 15, except that data word are stored in a manner supporting little-endian or big-endian format.

However, Rezeanu teaches a memory array that can stored data in either big-endian format or little-endian format (col. 3, lines 30-35, and col. 4, lines 14-17).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Rezeanu in combination with the method as taught by Baddiley in order to reduce time after data is fetched, reduce expensive circuit and power consumption (col. 1, lines 28-35).

10. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno (U.S. Patent No. 6,105,114) in view of Blankenship (U.S. Patent No. 5,680,365).

Referring to claim 31, as applied to claim 16, Okuno teaches all the limitations of claim 31 except that data inputs and data outputs share a common bus.

However, Blankenship teaches a dual port memory comprising a memory cell array including a plurality of memory cells arranged in rows and columns, first and second

input/output ports for inputting/outputting data to/from the memory device with each port including a data terminal, read/write amplifiers connected to the storage buffer for reading data from the memory cell array to the storage buffer and writing data from the storage buffer to the memory cell array. A common global input/output bus is connected to the read/write amplifiers of the first and second ports, and to the memory cell array (col. 3, lines 3-17).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Blankenship in combination with the method as taught by Okuno so that read and write operations are carried out at high speed (col. 2, lines 63-65).

11. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno (U.S. Patent No. 6,105,114) in view of Tanaka (U.S. Patent No. 4,728,929).

Referring to claim 36, as cited above, Okuno teaches all the limitations of claim 36, except that inputs are converted to 1's complement format.

However, converting input data to 1's complement format is common in the art as described in US Patent No. 4,728,929 to Tanaka, which discloses a circuit for converting inputs into 1's complement format (col. 10, lines 11-19).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Tanaka in combination with the method as taught by Okuno in order to store negative values (col. 10, lines 11-19).

12. Claim 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno (U.S. Patent No. 6,105,114) in view of Clark et al. (U.S. Patent No. 6,603,814).

Referring to claims 35 and 37, as applied to claim 16 above, Okuno teaches all the limitations of claims 35 and 37, except for data input and output is provided in 2's complement format.

However, Clark et al. teach a method for storing video data, wherein as shown in Fig. 2, video signals 202, a discrete wavelet transform 204 block. The video compressor 200 also comprises a signed magnitude converter 210. In practice, the wavelet coefficients are stored in the input storage area 206 using a data representation that is most conducive to simple math operations, e.g., a one's complement or two's complement data representation (col. 5, lines 58-67, and col. 6, lines 1-3).

Therefore, it would have been obvious to one skilled in the to utilize the method as taught by Clark et al. in combination with the method as taught by Okuno in order to avoid picture degradation (col. 2, lines 55-58).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

10/10/2003

Matthew C. Bella

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